NAMEOFTHE FACULTY : Promila Hansu

DISCIPLINE : Computer Engineering

SEMESTER : 3rd

SUBJECT : DIGITAL ELECTRONICS

LESSON PLAN DURATION : 15weeks

WORK LOAD PER WEEK(INHOURS) : LECTURE-03,PRACTIACL-04

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| WEEKS.N. | THEORY | |
| LectureHours | TOPIC  (Including Assignment/Test) | Experiment |
| 1st | 1 | Introduction to Digital Electronics: Distinction between analog and digital signal. | Verification and interpretation of truth tables for AND,OR,NOTNAND,NORandExclusiveOR(EXOR)  and Exclusive NOR(EXNOR)gates |
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| 2 | Applications and advantages of digital signals. |
| Verification and interpretation of truth tables for AND,OR,NOTNAND,NORandExclusiveOR(EXOR)  andExclusiveNOR(EXNOR)gates |
| 3 | Number System:Binary,octaland hexadecimal number system |
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| 2nd | 4 | Conversion from decimal land hexadecimal to binary and vice-versa. | Verification and interpretation of truth tables for AND,OR,NOTNAND,NORandExclusiveOR(EXOR)  and Exclusive NOR(EXNOR)gates |
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| 5 | Binary addition and subtraction including binary points. 1’s and 2’s complement method of addition/ subtraction |
| Verification and interpretation of truth tables for AND,OR,NOTNAND,NORandExclusiveOR(EXOR)  and Exclusive NOR(EXNOR)gates |
| 6 | Codes andParity:Conceptofcode, weighted and non-weighted codes |
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| 3rd | 7 | Examplesof8421,BCD,excess-3andGray code | Realization of logic functions with the help of NAND or NOR gates |
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| 8 | Conceptofparity,singleanddoubleparity and error detection |
| Realization of logic functions with the help of NAND or NOR gates |
| 9 | LogicGatesand Families: Conceptof negative and positive logic. |
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| 4th | 10 | Definition,symbolsandtruthtablesofNOT, AND, OR Gates | To design a half adder using XOR and NAND gates and verification of its operation |
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| 11 | Definition,symbolsandtruthtablesof NAND, NOR, EXOR Gates |
| To design a half adder using XOR and NAND gates and verification of its operation |
| 12 | Definition,symbolsandtruthtablesofNAND and NOR as universal gates. |
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| 5th | 13 | Introduction to TTL and CMOS logic families | Construction of a full adder circuit using XOR and NAND gates and verify its operation |
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| 14 | Assignment-1 |

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| 5th |  |  | Construction of a full adder circuit using XOR and NAND gates and verify its operation |
| 15 | SessionalTest-1 |
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| 6th | 16 | Logic Simplification: Postulates of Boolean algebra, De Morgan’s Theorems | Revision Experiment Performed |
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| 17 | Implementation of Boolean (logic)equation with gates |
| Revision Experiment Performed |
| 18 | K-Map(upto 4variables) |
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| 7th | 19 | Simple application in developing combinational logic circuits | Verification of truth table for positive edge triggered,negativeedgetriggered,leveltriggered ICflip-flops(AtleastoneICeachofDlatch,Dflip- flop, JK flip-flops |
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| 20 | Arithmetic circuits:Half adder andFull adder circuit |
| Verification of truth table for positive edge triggered,negativeedgetriggered,leveltriggered ICflip-flops(AtleastoneICeachofDlatch,Dflip- flop, JK flip-flops |
| 21 | Halfadder and Fulladder circuit,designand implementation |
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| 8th | 22 | Decoders,Multiplexers,Multiplexersand Encoder: Introduction | Verification of truthtable for encoder and decoder ICs, Mux and DeMux |
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| 23 | Fourbitdecodercircuitsfor7segment display and decoder/driver ICs |
| Verification of truthtable for encoder and decoder ICs, Mux and DeMux |
| 24 | Basic functions and block diagram of MUX and DEMUX with different ICs |
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| 9th | 25 | Basic function sandblockdiagramof Encoder | To design a 4 bit SISO, SIPO, PISO, PIPO shift registersusingJK/Dflipflopsandverificationof theiroperation |
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| 26 | Latches and flipflops:Conceptandtypesof latch with their working and applications |
| To design a 4 bit SISO, SIPO, PISO, PIPO shift registersusingJK/Dflipflopsandverificationof theiroperation |
| 27 | Operation using waveforms and truth tables of RS, T, D and Master/Slave JK flip flops. |
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| 10th | 28 | Difference between a latch and a flipflop. | Revision Experiment Performed |
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| 29 | Assignment-2 |
| Revision Experiment Performed |
| 30 | SessionalTest-2 |
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| 11th | 31 | Counters: Introduction | Todesigna4bitringcounterandverifyits operation |
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| 32 | Introduction to Asynchronous counters |
| Todesigna4bitringcounterandverifyits operation |
| 33 | Introduction to Synchronous counters |
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| 12th | 34 | Binary counters | Use of Asynchronous CounterICs (7490or7493) |
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| 35 | Divide by Nripple counters |
| Use of Asynchronous CounterICs (7490or7493) |
| 36 | Decade counter,Ringcounter |
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| 13th | 37 | Shift Register: Introduction and basic concepts including shift left and shift right. Serial in parallel out, serial in serial out | To design and verification of A/D Converter |
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| 38 | Parallelin serialout,parallelin parallelout. Universal shift register. |
| To design and verification of A/D Converter |
| 39 | A/D and D/A Converters: Working principle of A/D and D/A converters, Stair step Ramp A/D converter, Dual Slope A/D converter. |
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| 14th | 40 | Successive Approximation A/D Converter, detail study of Binary Weighted D/A converter, R/2R ladder D/A converter. Applications of A/D and D/A converter | To design and verification of D/A Converter |
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| 41 | Semiconductor Memories: Memory organization,classification of Semiconductor memories |
| To design and verification of D/A Converter |
| 42 | (RAM,ROM,PROM,EPROM,EEPROM),  Static and dynamicRAM |
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| 15th | 43 | Introductionto74181ALUIC | To design and verification of 74181 ALU IC |
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| 44 | Assignment-3 |
| To design and verification of 74181 ALU IC |
| 45 | SessionalTest-3 |
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